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ESD effects in capacitive RF MEMS switches

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ABSTRACT

RF MEMS have shown very attractive characteristics in automotive, communication, aeronautic and aerospace applications, thanks to its low mass and volume, low losses, low power consumption, high isolation and a wide operative frequency range. Moreover they have demonstrated good integration with electronics which show their ability to built-in innovative RF architectures [1]. Nevertheless the air gap between the suspended membrane and the bottom electrode is very close and the geometries lead to non-uniform high electric field, so they could be very sensitive according to electrostatic discharges (ESD), overvoltage, charging, or corona effects. Besides the fact they integrate moving parts, air gaps or cavities complicate the analogy with traditional CMOS electronics. To date there is only a few papers dealing with this issue [2,3,4], which should be further investigate in order to understand or model the physic of failure related to ESD stresses.

This paper is dedicated to failure analysis of capacitive RF MEMS under ESD stresses. The experiments were performed on LAAS designed-switches from ISIT-FHG Multi-Process-Wafer run of AMICOM, as presented in Fig. 1.

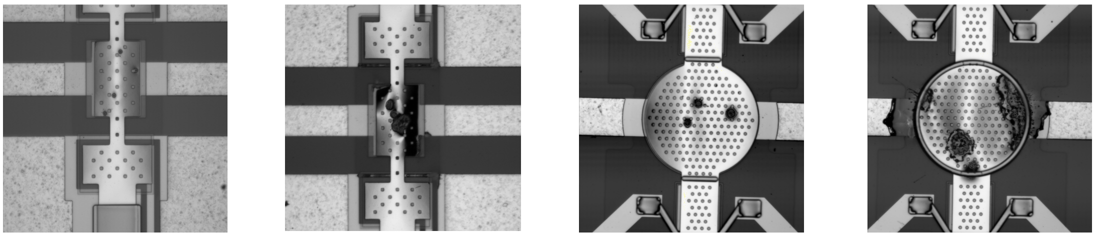
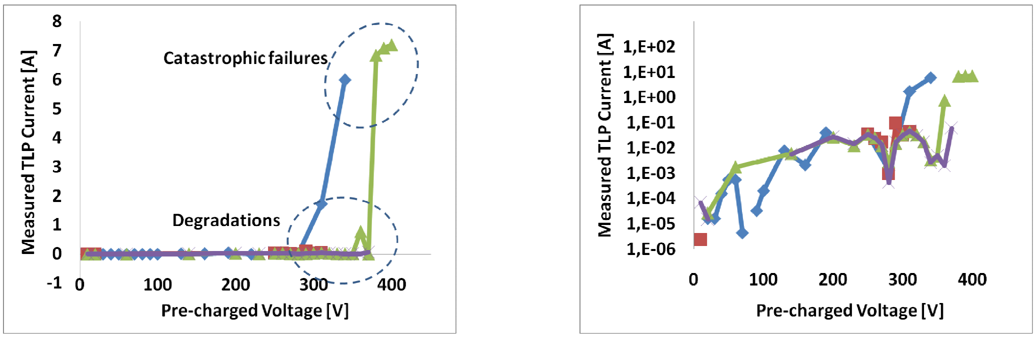

a) b) c) d)

Fig. 1. Capacitive RF MEMS switches submitted to ESD stresses, a) and c) damaged switches, b) and d) after catastrophic failure.

Those devices, with aluminum nitride as dielectric have been experimented through a 100ns Transmission Line Pulsing (TLP) bench set, commonly used for evaluation of ESD robustness in integrated circuits. TLP pulses were applied between the signal line and the ground with the membrane in the up-state position. The devices functionalities are monitored by a microscope (Fig. 1) and current-voltage curves have been extracted

(Fig. 2). The TLP voltage magnitude range from 10 to 420 V were sequentially generated. For voltage around 300V we can observe (Fig. 2.a) a current transfer between the electrodes which can refer to micro-electric arc effects corresponding to visible hot spots showed in Fig. 1.a. and Fig. 1.c. Even in this case, scattering parameters measurements have been carried out to justify the switches functionalities.



a) b)

Fig. 2. TLP I-V characteristics of the switches, a) normal scale, b) logarithmic scale

Catastrophic failures occurs when we keep increasing the magnitude (Fig. 2.a) and the corresponding consequences are shown in Fig. 1.b and Fig. 1.d. In order to know what happened before the degradations, Fig. 2.b. plots the current-voltage graphic in a logarithmic scale and some transient phenomenon can be observed, probably due to large leakage current and charge traps [3]. To deepen the analysis, the next step of this work consist in an contact-less capacitance-voltage (C-V) characteristic, ESD charging study. In fact, Fig.3. presents the C-V characteristic below pull-in.

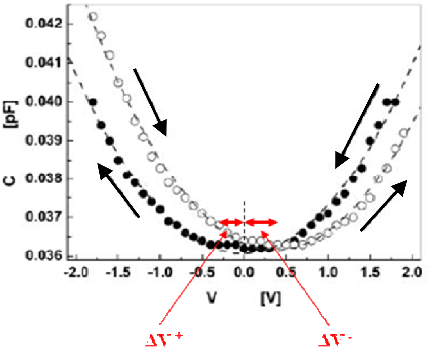


Fig. 3. Contact-less capacitance-voltage characteristics

Depending on the polarity of characteristic starting bias the capacitance minimum is observed at opposite polarity. This is caused because an opposite charge is induced at dielectric surface and the electrostatic force is minimized when both the bridge and the dielectric have the same net charge, which is the minimum electric field [5]. Due to charge injection the opposite effect takes place when the C-V characteristic is dawn beyond pull-in.

This paper presents the reliability behavior of capacitive RF-MEMS through ESD stresses by means of a TLP method.

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