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TOPOLOGY OPTIMIZATION FOR NANO-SCALE HEAT TRANSFER

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ABSTRACT

Owing to the advances in manufacturing processes and infrastracture, heat conduction at nano-scales has received increasing attention in the recent years; see for example the monographs [1, 2] and references therein. One of the main drivers for such an interest is the continuing miniaturization of micro-electronic devices involving low-conductivity semiconductors and dielectrics. The thermal management in such devices becomes a crucial factor, in many cases being the "bottleneck" limiting the performance of the device or even leading to accelerated failure of the device [3, 4, 5].

At length scales ranging from hundreds of nanometers to just a few microns (referred to as nano-scales in this paper) Fourier's law of heat conduction observed at macro-scales is no longer valid [6], which is not unexpected considering the fact that the Fourier relation is based on empirical macroscopic evidence and does not explicitly describe the relevant transport mechanisms. To appropriately model modern miniature devices we have to explicitly account for the fact that the temperature in solids is a measure of average energy of microscopic motions of atoms around their sites [1]. The quantum of such vibrational energy is called a phonon [7]. While inherently being wave phenomena, phonons can be thought of as particles (i.e., their phase information may be discarded) as long as the length-scales of interest are larger than the characteristic wave-length, which is true for all but the tiniest of devices. For example, at room temperature the characteristic wave-length of heat carrying phonons is of the order of only $1nm$.

In conducting solids heat is transported by both phonons and electrons, whereas in low-conductivity semiconductors and dielectrics, heat is almost exclusively carried by phonons (atomic vibrations) [1]. Tracking every individual atom movement is a computationally prohibitive task. For example, state-of-the-art molecular dynamics simulations can deal with up to $1 \cdot 10^8$ atoms, corresponding to about $1/6$ of an average distance travelled by a phonon between collisions with other phonons in a silicon crystal at room temperature, the latter being approximately $3 \cdot 10^{-7} m$. To analyse and design larger structures of practical relevance we can employ kinetic theory to obtain the distribution of phonons in the system in a statistical sense. Such an approach is especially attractive since we are interested in a description of the performance of the system in terms of the statistical moments, the most important for heat-conduction problems being the system's temperature.

We are concerned with solving the phonon Boltzmann equations describing the statistical distribution of phonons in a given system only to a lesser degree; of major interest for us is the possibility of utilizing the kinetic theory for optimal design and synthesis of heat conducting systems at nano-scales. Namely, assuming that positions and intensities of heat sources and sinks are given, we distribute two materials in order to minimize a given temperature-dependent performance functional while satisfying certain prescribed requirements, or constraints. For example, manufacturing constraints may restrict the minimal feature size for all feasible designs/material distributions.

If the minimal feature size of feasible material distributions exceeds the mean free path of heat carriers (phonons, electrons) for the expected operating conditions by several orders of magnitude, empirical Fourier's law still provides an accurate macroscopic description of the underlying physical phenomena [1]. At room temperatures, this assumption is verified for most but nano-scale applications. Therefore, previous studies addressing the optimal design problems in heat conduction (see, e.g., recent papers [8, 9, 10] among many others as well as [11] and references therein) are not applicable to the situation at hand.

We illustrate the feasibility of the kinetic theory approach to topology optimization of heat conducting devices at nano-scales. In order to solve realistic relevant problems, a parallel high-performance implementation of this approach is absolutely imperative.

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